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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/042,464
Filing Date: January 08, 2002
Appellant(s): COENEN, MARTINUS JACOBUS

Michael Ure
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed July 30, 2007 appealing from the Office action mailed February 27, 2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5740087	Smentek et al.	4-1998

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Smentek et al., US Patent 5740087, hereinafter Smentek.

3. In re claims 1 and 2, Smentek discloses a method of and means for power management in a digital processing apparatus [col.1, ll.6-11], comprising [col.4, ll.27-47; fig.3 embodiment similar to fig.1 with primary difference of 374 and 384 used for generation of free running/ continuous sub clocks]:

- Receiving a continuously free-running master clock signal [370] [col.3, ll.29-51; col.5, ll.4-7] and means therefor.
- Generating a plurality of sub-clocking signals [triggering pulses] from said master clock signal and means therefor, wherein said plurality of sub-clocking signals change from a power-up rest condition to a continuously free running condition one at a time, following an initial switch-on of said digital processing apparatus (30) [col.5, ll.8-20; col.6, ll.20-26; data value in 384 set to 7 with dummy start asserted continuously to trigger continuously free running sub clocking signals].

4. As to claim 3, Smentek discloses, wherein each sub-clocking signal is used to clock a separate data processing part [functional block] of the apparatus [col.2, l.65 – col.3, l.28; col.6, ll.20-26].

5. As to claim 4, Smentek discloses, wherein each data processing part comprises circuitry [combinational logic, state machines] for processing a particular serial data bit or bits of a data word [col.2, l.65 – col.3, l.28].

6. As to claim 5, Smentek discloses, wherein said digital signal processing apparatus has a particular maximum data width and wherein said plurality of sub-clocking signals corresponds to said maximum data width [col.3, ll.19-28; maximum data width is processed completely by pipeline].

7. As to claim 6, Smentek discloses, wherein during a switch-off phase of said digital processing apparatus, said plurality of sub-clocking signals change from a continuously free running condition to a rest condition one at a time [fig.2; col.3, l.29 – col.4, l.26; start propagates down chain and disabling trailing functional blocks].

8. As to claim 7, Smentek discloses wherein said means for receiving a master clocking signal and generating a plurality of sub-clocking signals comprise:

- A shift register [latches 146-160] for providing a plurality of enabling signals, said plurality of enabling signals each changing from a non-active rest condition to an active normal condition and thereafter remaining at said active normal condition, said plurality of enable signals changing from the rest condition to the normal condition one at a time at predetermined time intervals following the initial switch on [col.3, l.29 – col.4, l.47].
- Logic circuitry [114] for receiving the enable signals and sequentially enabling the production of the sub-clocking signals [col.3, l.29 – col.4, l.47].

9. As to claim 8, Smentek discloses, wherein the logic circuitry comprises means [e.g., 147, 149] for ANDing respective enable signals with the master clock [fig.1; col.3, l.29 – col.4, l.47].

10. As to claim 9, Smentek discloses, wherein the logic circuitry comprises a number of AND gates corresponding to the number of enable signals, each AND gate having a first input for receiving its respective enable signal and a second input for receiving the master clocking signal, said sub-clocking signals being produced at the respective outputs of said AND gates [fig.1; col.3, l.29 – col.4, l.47].

11. In re claim 10, Smentek discloses a digital processing apparatus [digital system] [abstract] comprising:

- A device in accordance with the limitations as discussed above in reference to claim 2.
- A plurality of discrete data processing parts [functional blocks], each of said data processing parts being clocked by a respective one of said plurality of sub-clocking signals [col.2, l.65 – col.3, l.28].

(10) Response to Argument

Rejection of Claims 1-10 as Anticipated by Smentek

Applicant argues substantially that in Smentek, "there are no continuously free running sub-clock signals generated from a master clock". Examiner disagrees as the Smentek device shown in figure 3 clearly illustrates the means for generating continuously free running sub-clock signals [triggering pulses FIRE1, FIRE2...] from a master clock [370] by setting the data value in power control register 384 to 7 with dummy start asserted continuously for *full* power operation [col.6, ll.20-26]. It can be seen from figure 3 of Smentek that the FIREx sub-clocks are triggered by the OR results [376] of START [316] and DUMMY START [378] signals. The DUMMY START signal can be set to ***continuous*** assertion, resulting in a ***continuous*** ripple of triggered sub-clocks FIRE1, FIRE2... [col.6, ll.20-26; fig.5; with datavalue in 384 set to 7 for

full power] that would be identical to the continuously free running sub-clock signals as illustrated in figure 2 of Applicant's specification. Accordingly, Examiner submits that Smentek does disclose "continuously free running sub-clock signals generated from a master clock".

Applicant argues that "the timing diagram shown in Figure 2 of Smentek... may be contrasted with Figure 2 of the present specification, showing continuously free running sub-clock signals..." Examiner respectfully points out that the timing diagram shown in figure 2 of Smentek does ***NOT*** represent the device of figure 3, but the *prior art device of* ***figure 1***. As a matter of fact, Smentek's device of figure 3 is used to solve the problems of prior art figure 1 [col.1, ll.43-50] by utilizing the DUMMY START signal to provide a ***continuous free running sub-clock signals*** for the pipeline stages [i.e., avoid thermal cycling].

Applicant argues that "the trigger pulses of Smentek would not be continuously free running because of the nature of the pipeline apparatus..." Examiner points to Applicant's admission that "each stage [of the pipeline] is clocked at a rate that is 1/N the rate of the master clock... respective stages are therefore, necessarily, gated in a 'one-shot' manner by the state machine 315" and submits that a pipeline clocked at 1/N the rate of the master clock [i.e., sub-clocks], gated in a "one-shot" manner would be ***continuously*** gated "one-shot" at a time as the ***continuous*** free-running sub-clocks arrive, with the superfluous results associated with the DUMMY START signals being ignored [col.5, ll.8-20].

As such, Examiner submits that Applicant's arguments are not persuasive and the rejections in view of Smentek are valid.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Tse Chen TWC

October 12, 2007

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